

PG142-B00

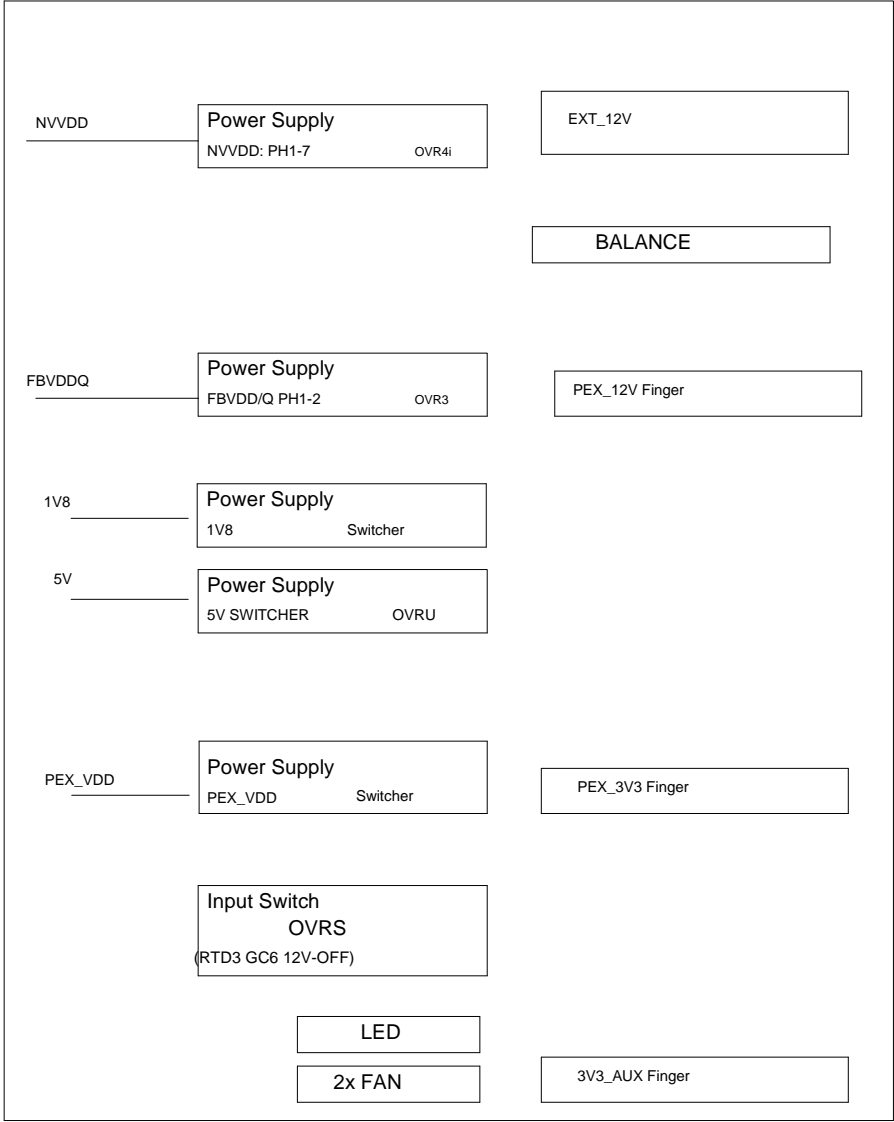
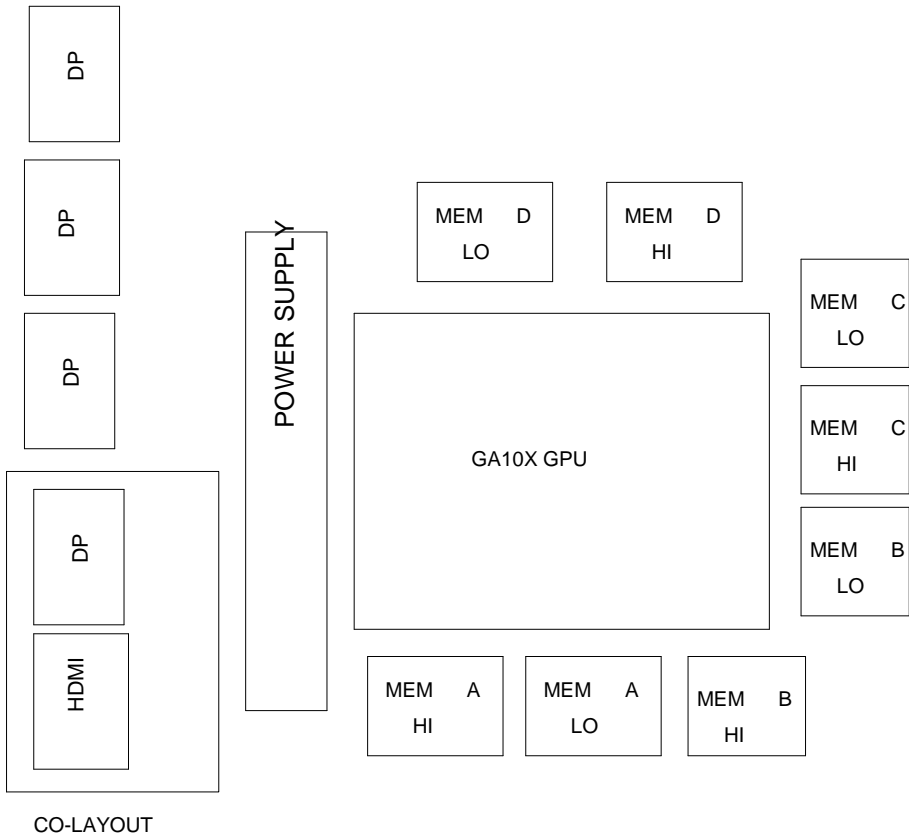
DP + DP + DP + HDMI/DP

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCIe GEN4 RC TERMINATIONS
5	MEMORY: GPU FB_AB
6	MEMORY: FBA[31:0]
7	MEMORY: FBA[63:32]
8	MEMORY: FBB[31:0]
9	MEMORY: FBB[63:32]
10	MEMORY: GPU FB_CD
11	MEMORY: FBC[31:0]
12	MEMORY: FBC[63:32]
13	MEMORY: FBD[31:0]
14	MEMORY: FBD[63:32]
15	GPU PWR & GND 1
16	GPU PWR & GND 2
17	GPU PWR & GND 3 (XVDD)
18	GPU DECOUPLING FBVDDQ
19	GPU DECOUPLING NVVDD
20	GPU DECOUPLING NVVDD
21	IO: IFPAB NC
22	IO: IFPF DP
23	IO: IFPE DP
24	IO: IFPD DP
25	IO: IFPC HDMI/DP

Page	Description
26	MISC1: ROM, XTAL, STRAPS
27	MISC2: JTAG, GPIO, ADC, I2C, FL, STEERO
28	MISC3: RGB
29	PS: 1V8
30	PS: 5V
31	PS: PEXVDD
32	PS: FBVDDQ
33	PS: FBVDDQ PH2
34	PS: NVVDD Controller
35	BLANK PAGE
36	PS: NVVDD PH4, PH6
37	PS: NVVDD PH1, PH3
38	PS: NVVDD PH2, PH5
39	PS: NVVDD PH9
40	PS: NVVDD PH7
41	PS: NVVDD PH10, PH8
42	PS: OVRS_INPUT POWER BALANCE
43	PS: RDT3_12V & 3V3_A Switcher
44	PS: INPUTS, FILTERING and MONITORING
45	PS: PEX_12V, PEX_3V3 AND A3V3_AUX
46	PS: STEERING, UPB, HOT UNPLUG
47	SEQ: 5V, 1V8, 3V3_SEQ
48	SEQ: NVVDD, PEX, FBVDDQ ENABLE
49	SEQ: MISC
50	SEQ: VOLTAGE MONITOR

Page	Description
51	FAN & LED
52	PS:OVRM_PWR_SENSE
53	MECH
54	PTC





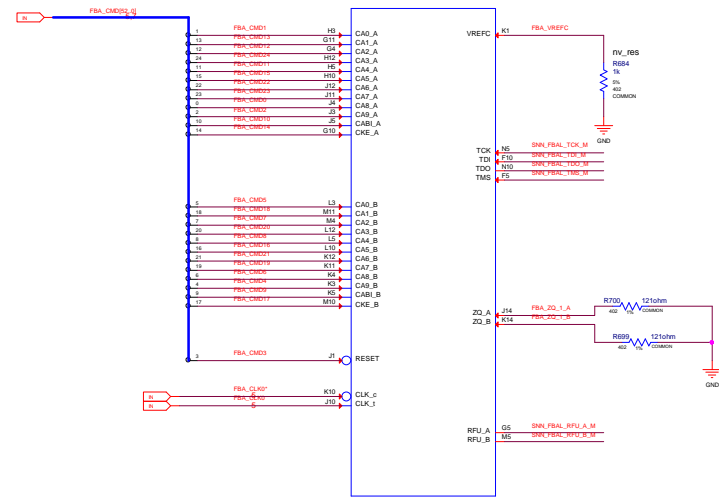
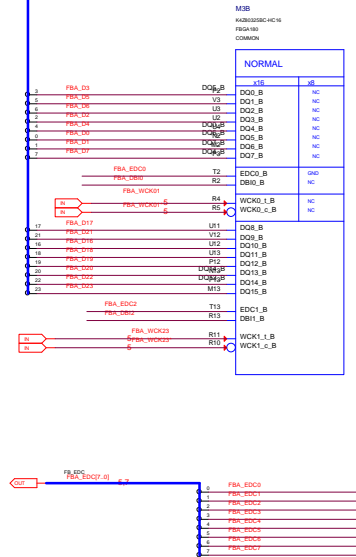
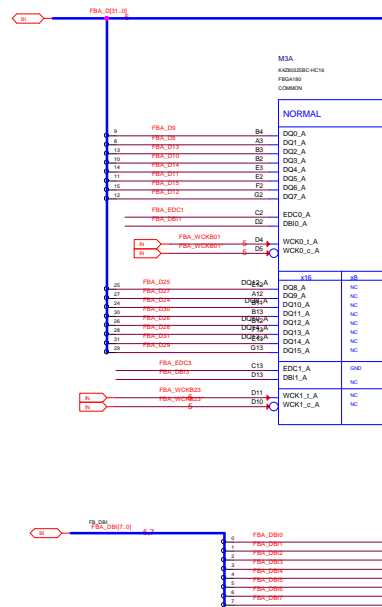
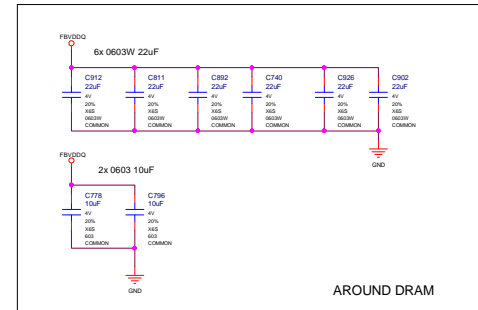
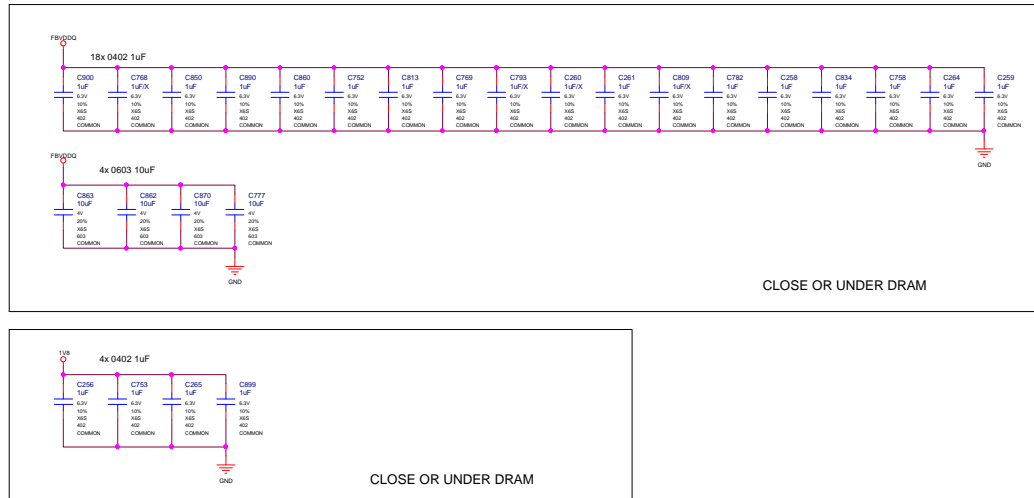
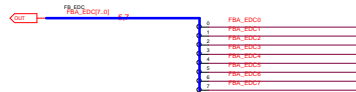
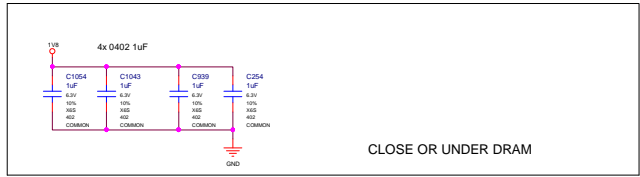
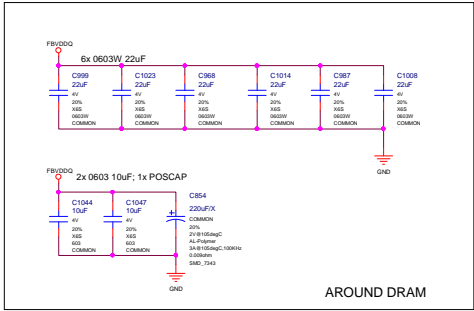
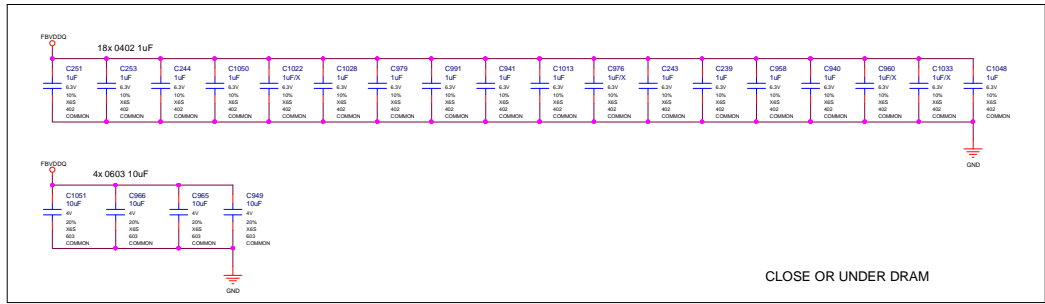
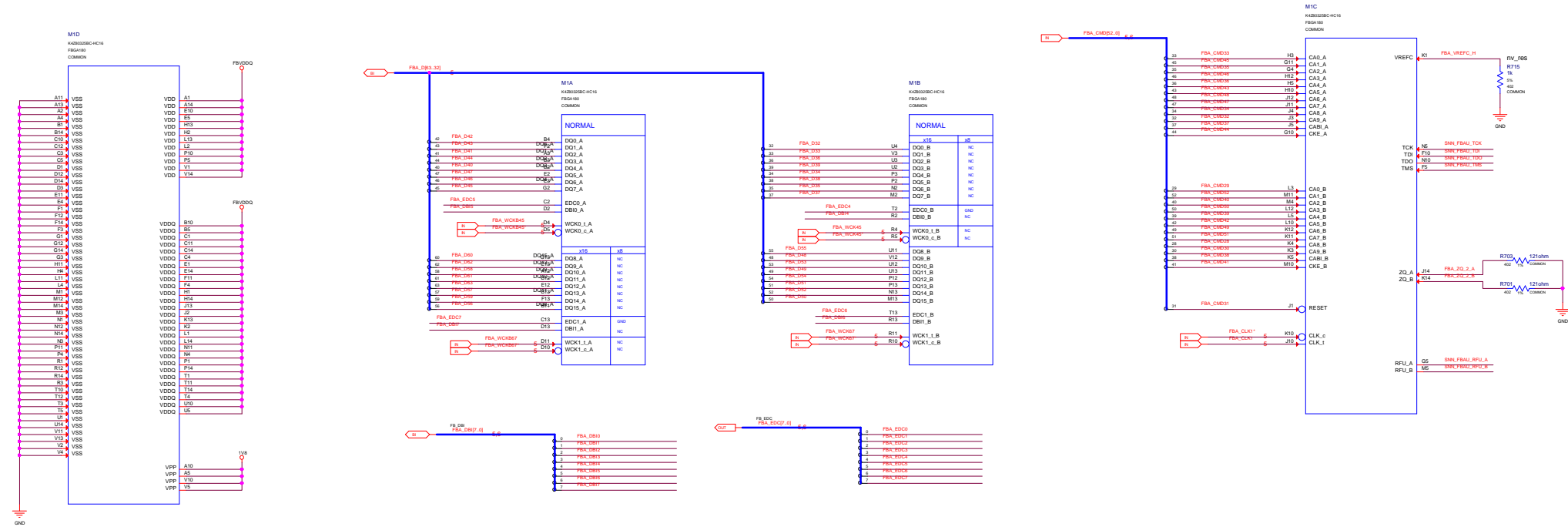
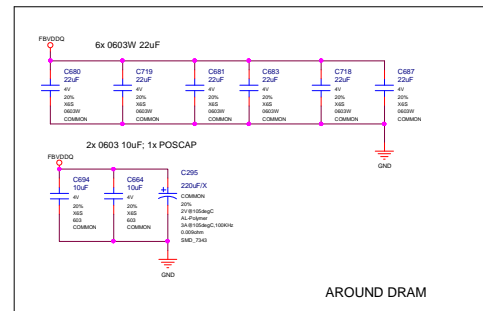
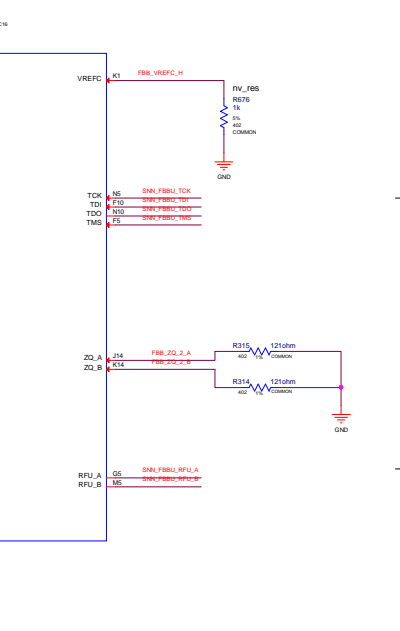


Diagram illustrating the network structure for FBA_DSB10. A red hexagon labeled "DS" is connected to a blue line labeled "FBA_DSB10[7,8]". This line then branches into seven parallel lines, each labeled with a number (1-7) and "FBA_DSB10".

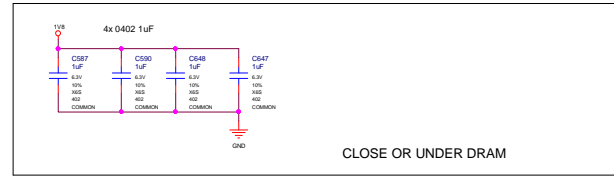
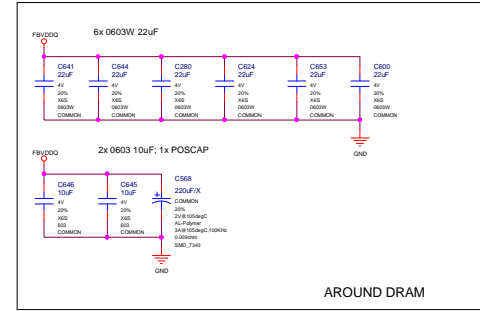
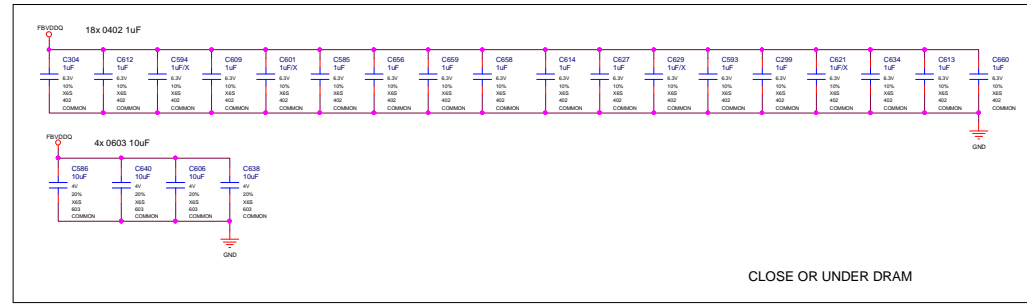
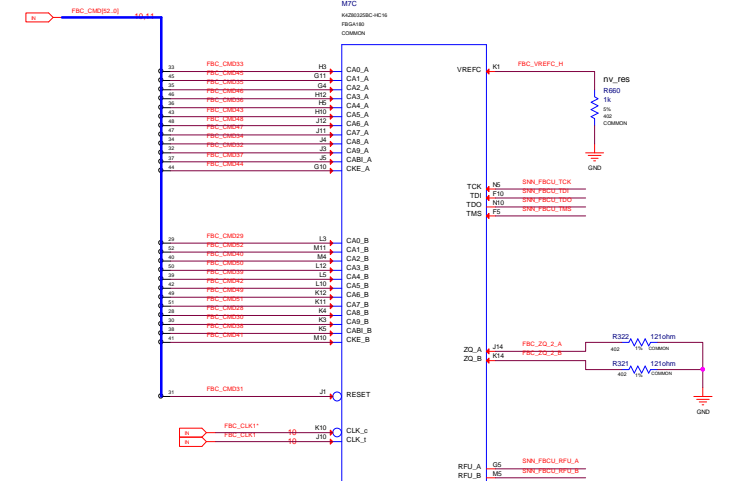
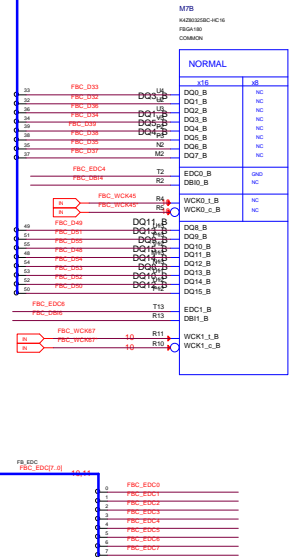
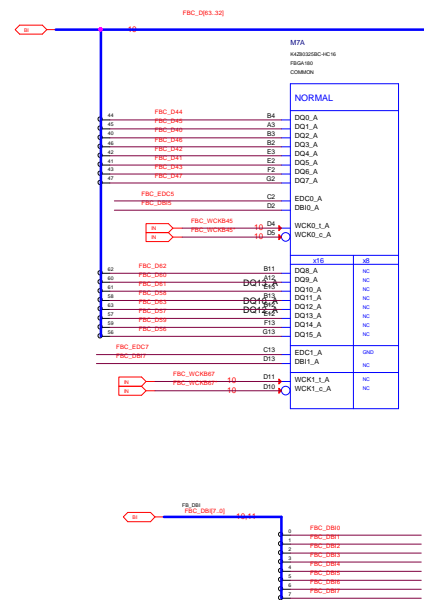
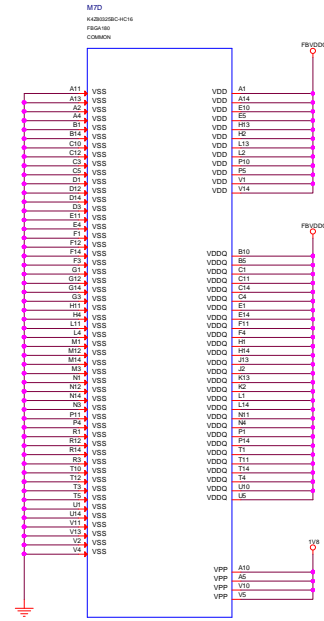


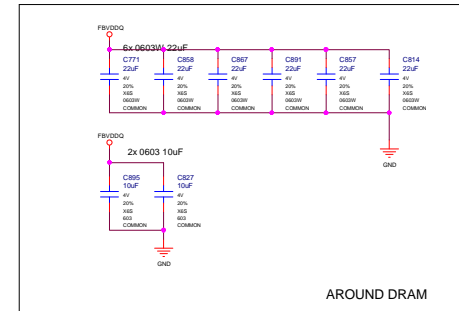
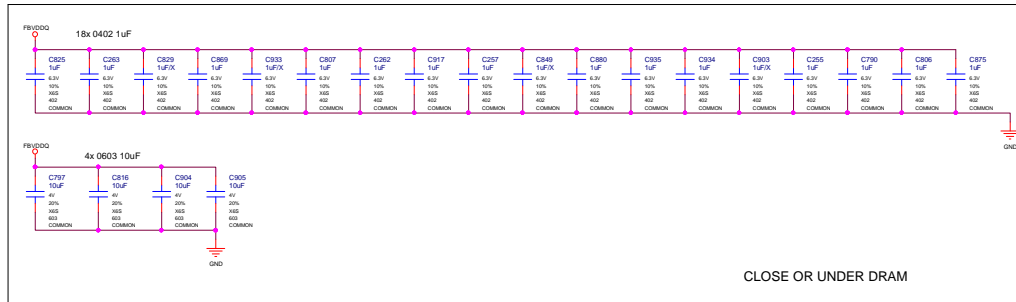
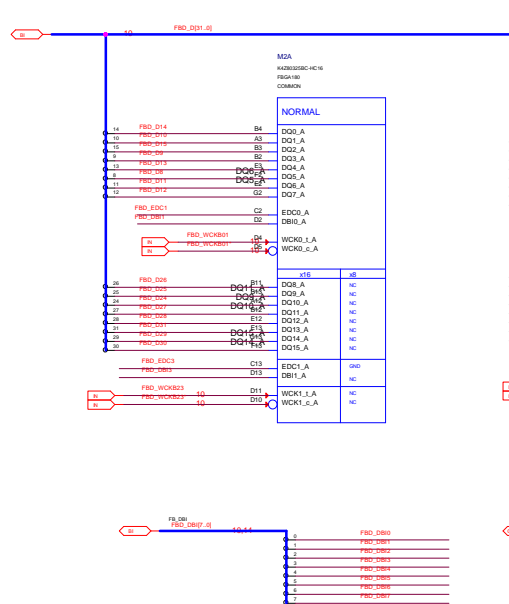




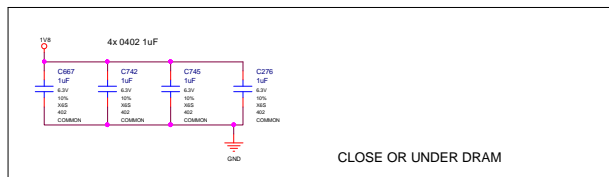
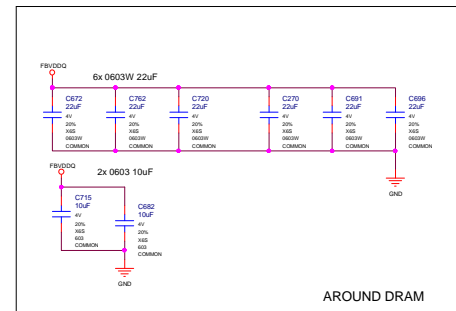
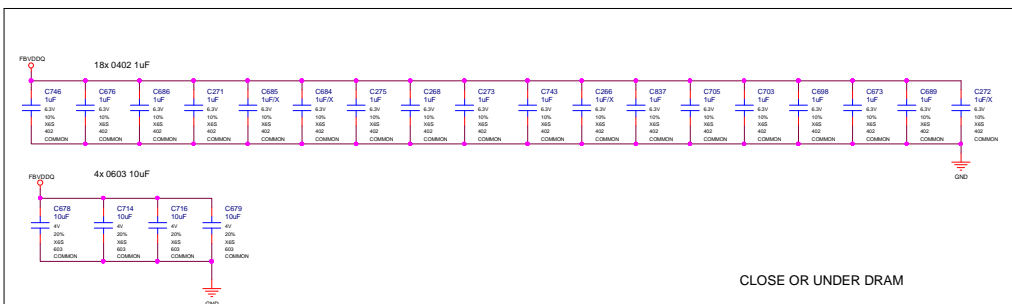
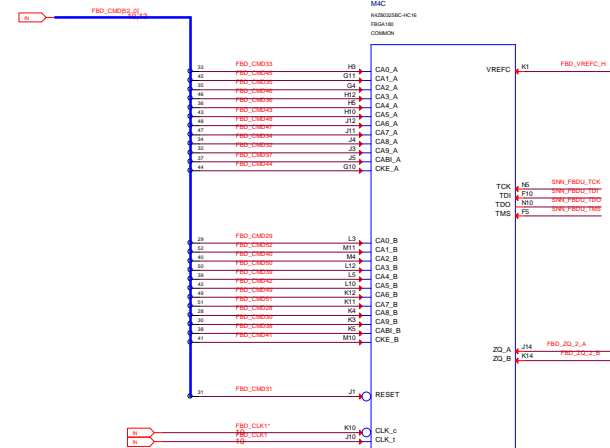
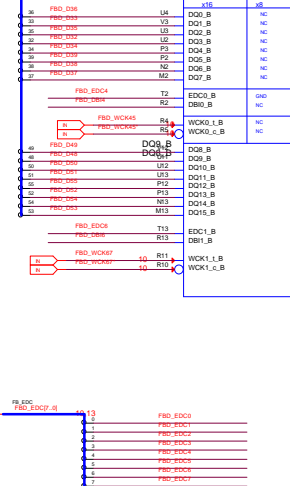
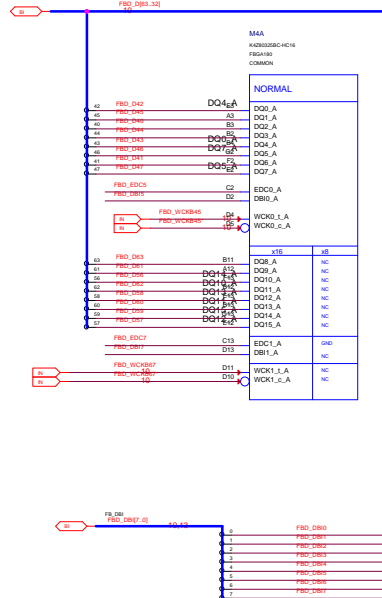


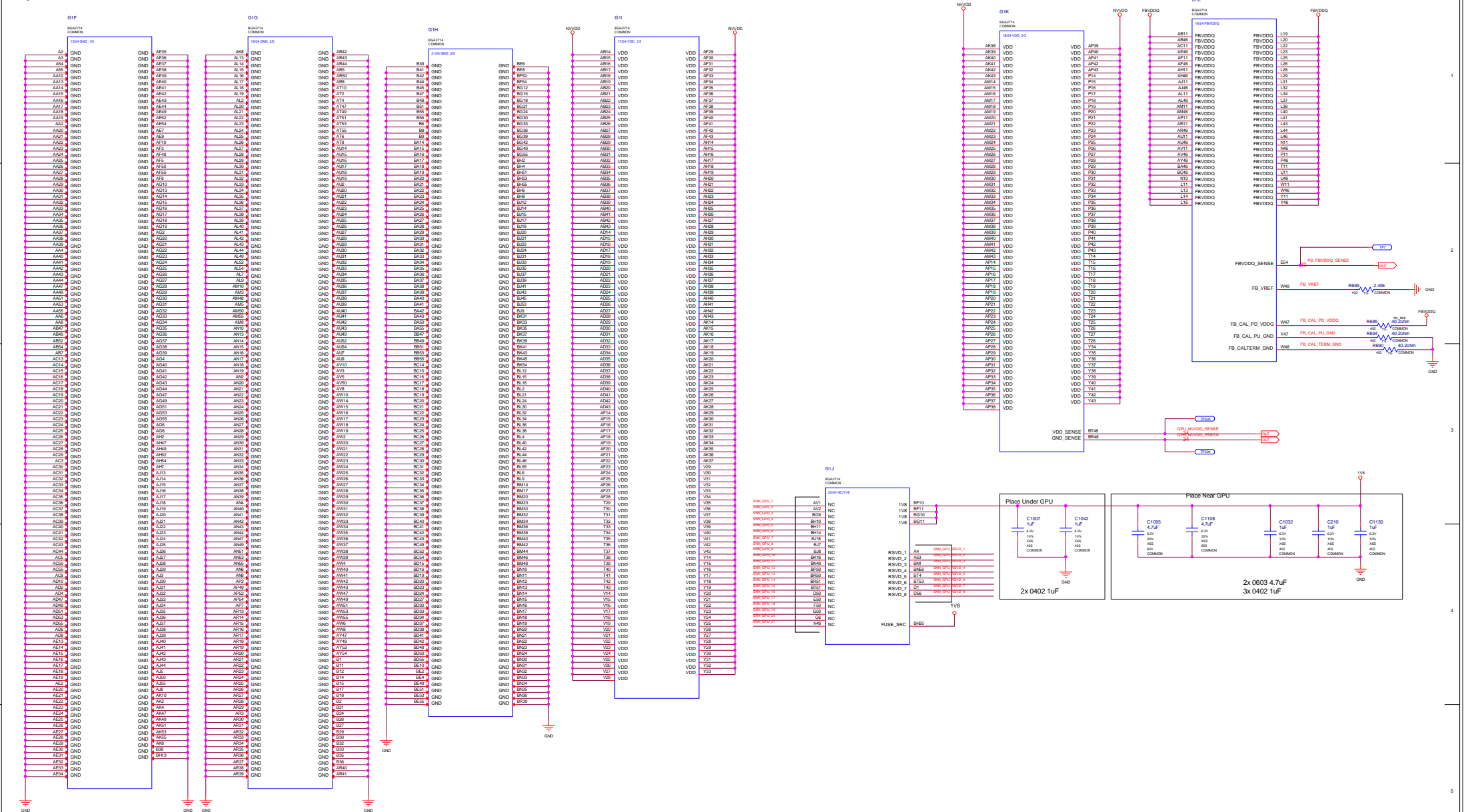


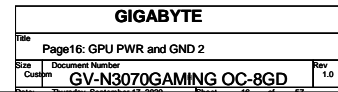


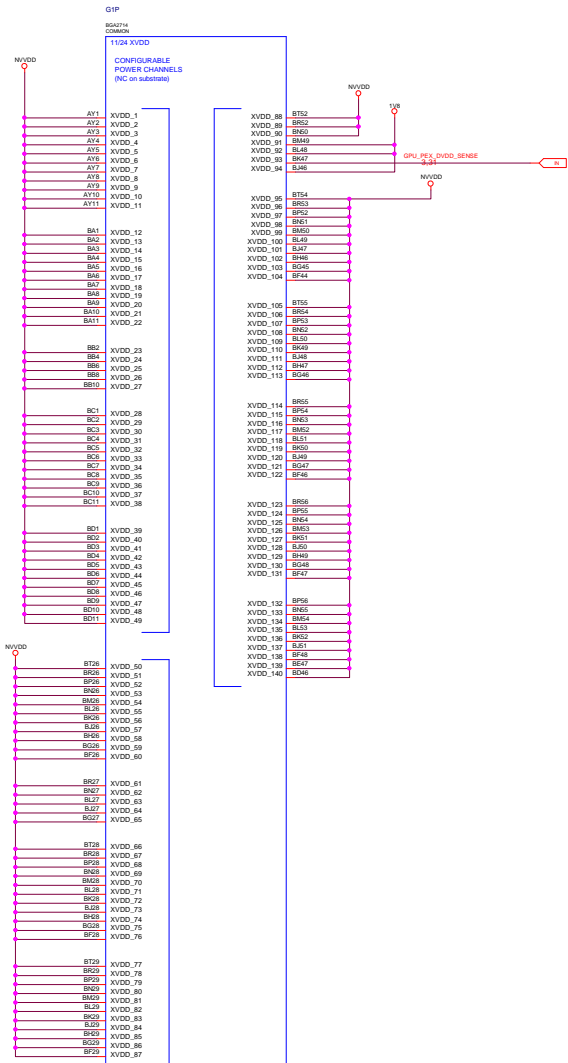


```
<ASSEMBLY_DESCRIPTION>
MEMORY: FBD[31:0]
```









FBVDDQ

FBVDDQ

UNDER GPU: 24x 0402 1uF; 8x 0603 10uF

Partition A

8x 1uF and 2x 10uF



Partition B

8x 1uF and 2x 10uF



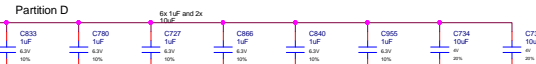
Partition C

8x 1uF and 2x 10uF



Partition D

8x 1uF and 2x 10uF



UNDER GPU

FBVDDQ

5x 0603 10uF; 9X 0603 22uF

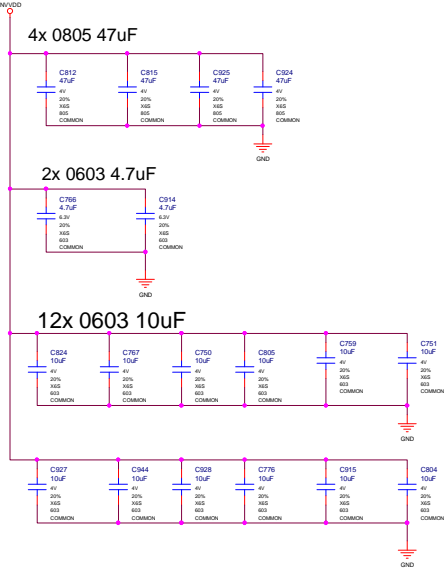
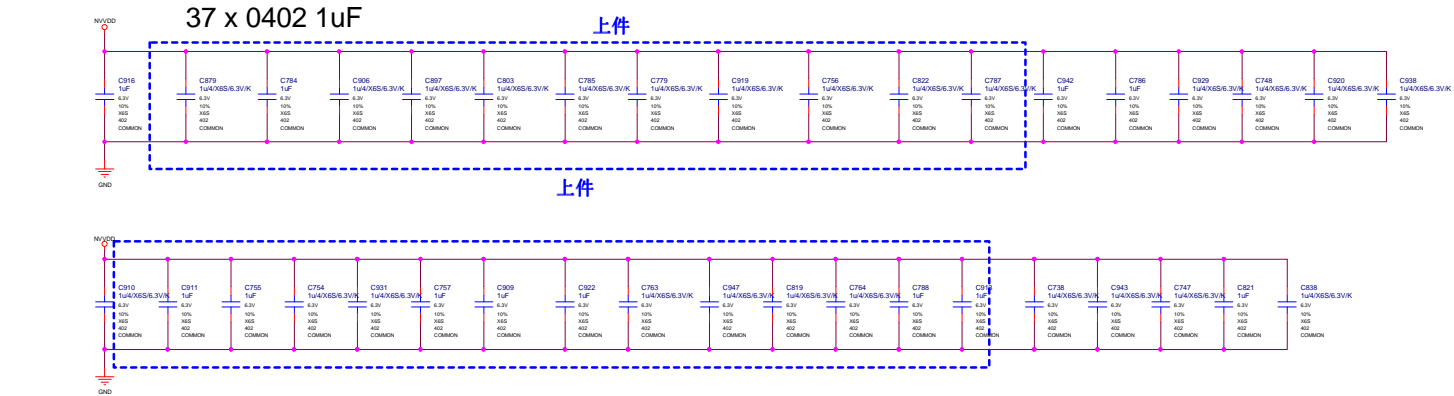
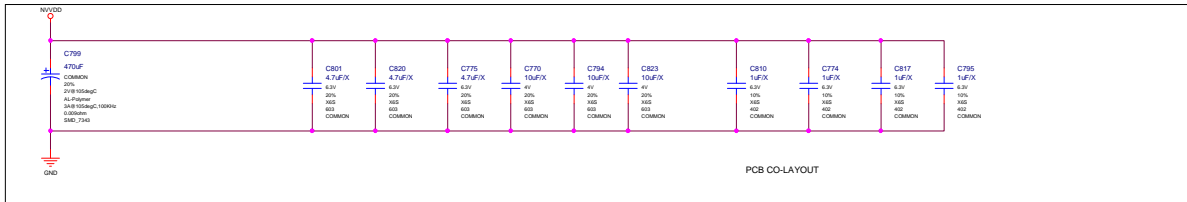
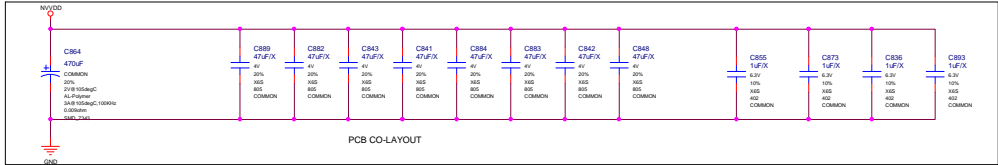
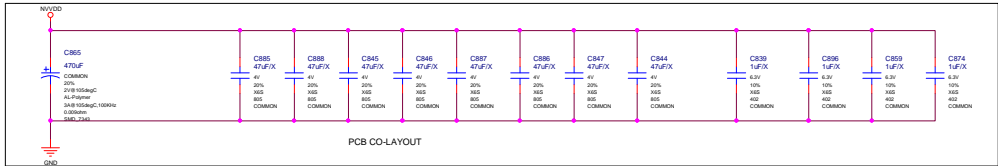
5x 10uF



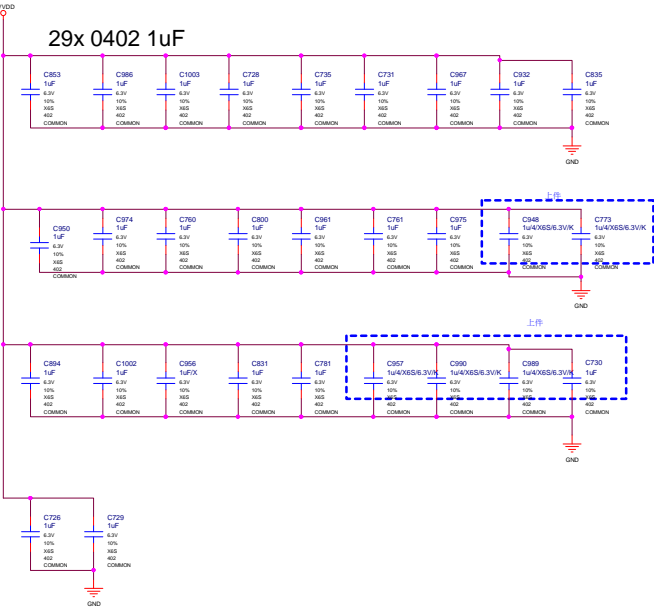
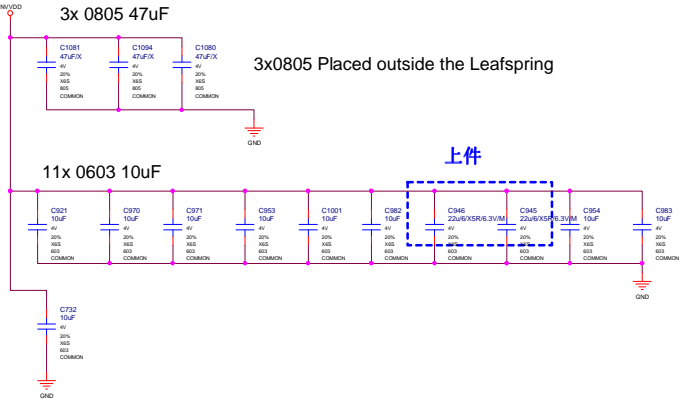
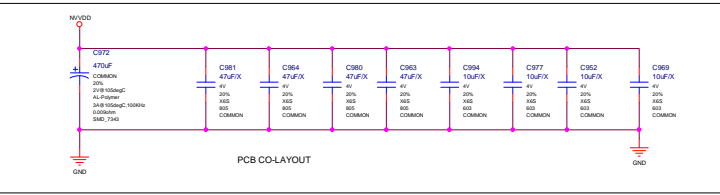
9x 22uF



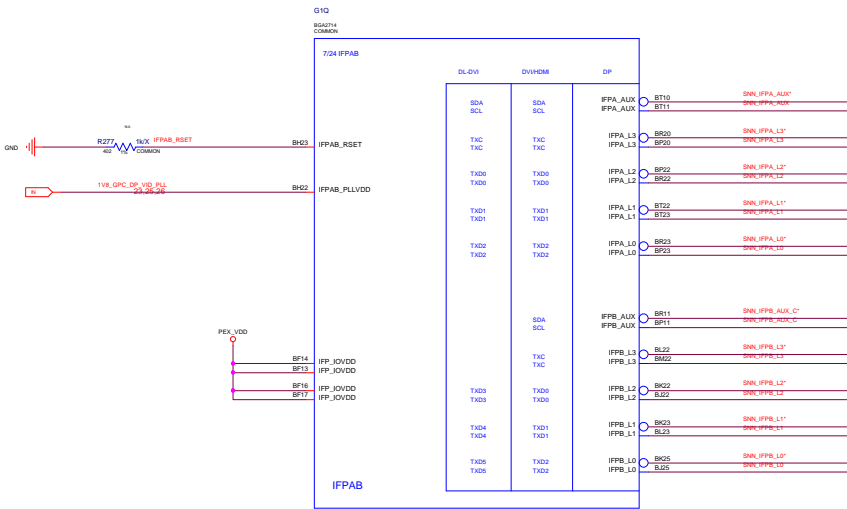
CLOSE TO GPU

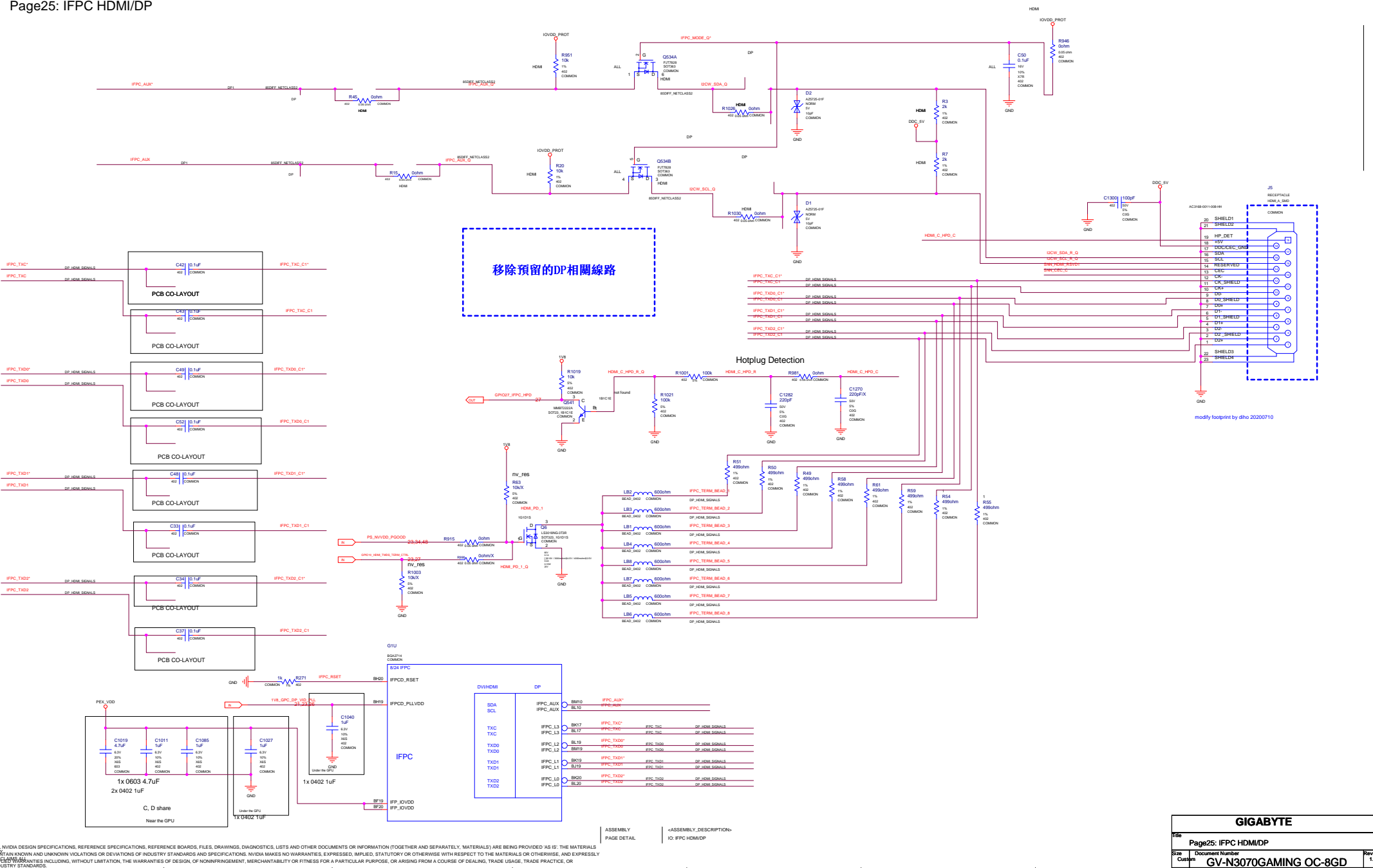


UNDER GPU



UNDER GPU





STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
TBD				

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1.ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

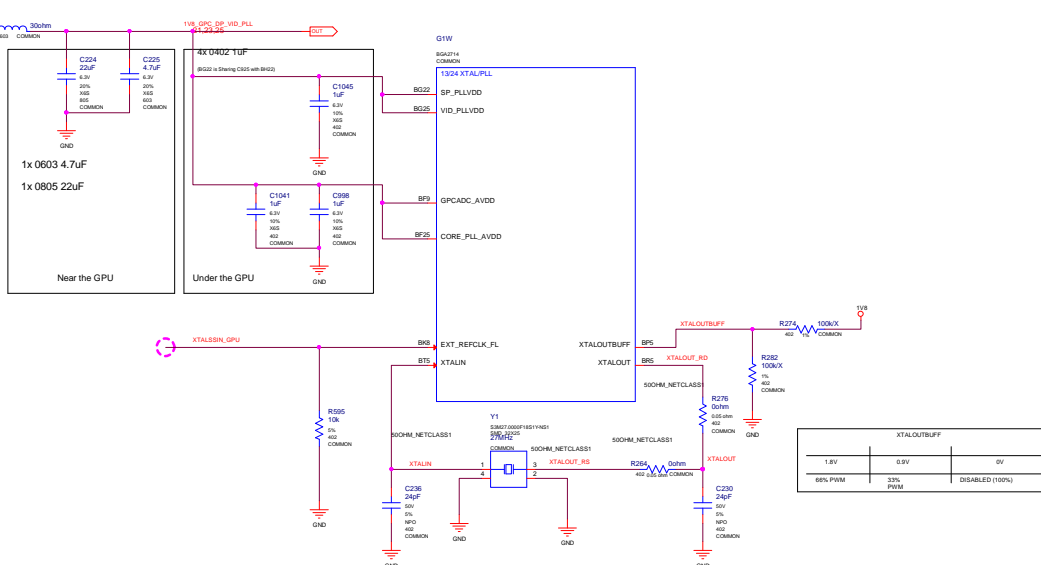
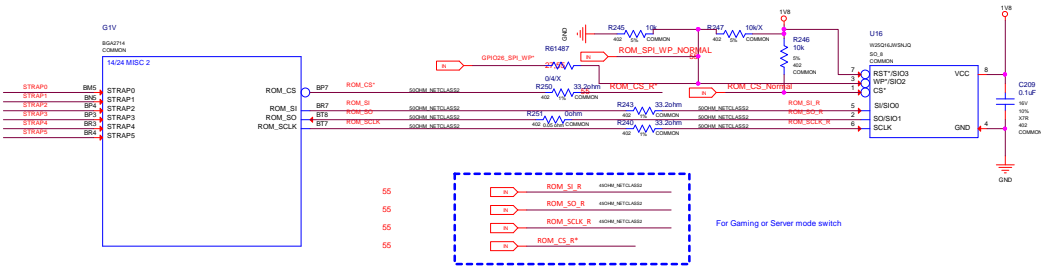
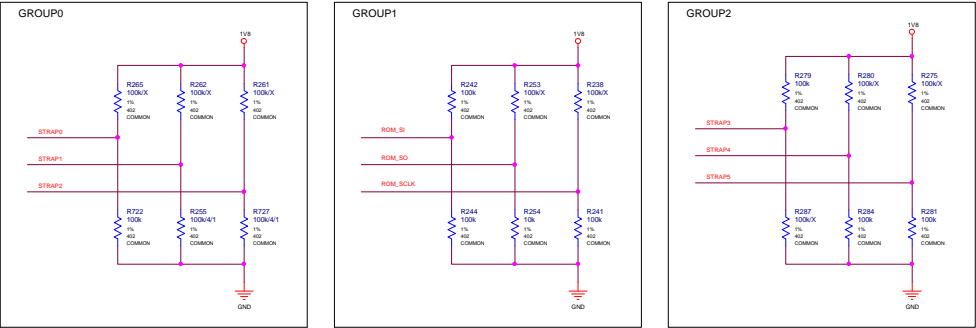
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

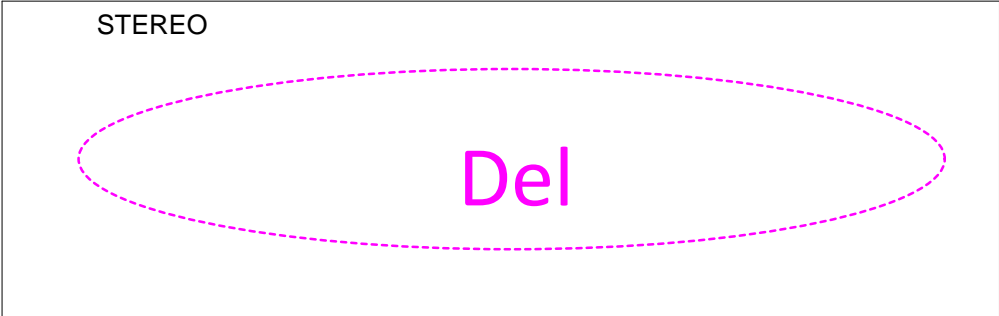
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





- 1: 12V
- 2: BLUE
- 3: GREEN
- 4: RED
- 5: WHITE

WHITE DRIVE

Del NV LED

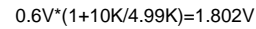
LOGO LED WHITE

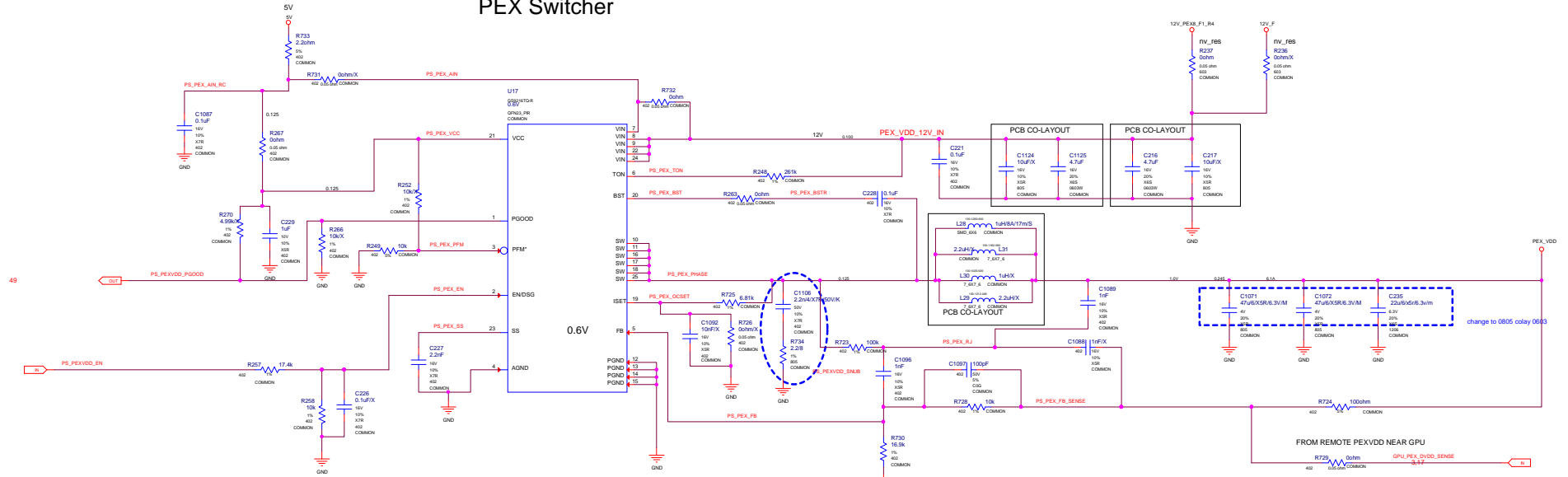
LOGO LED RED

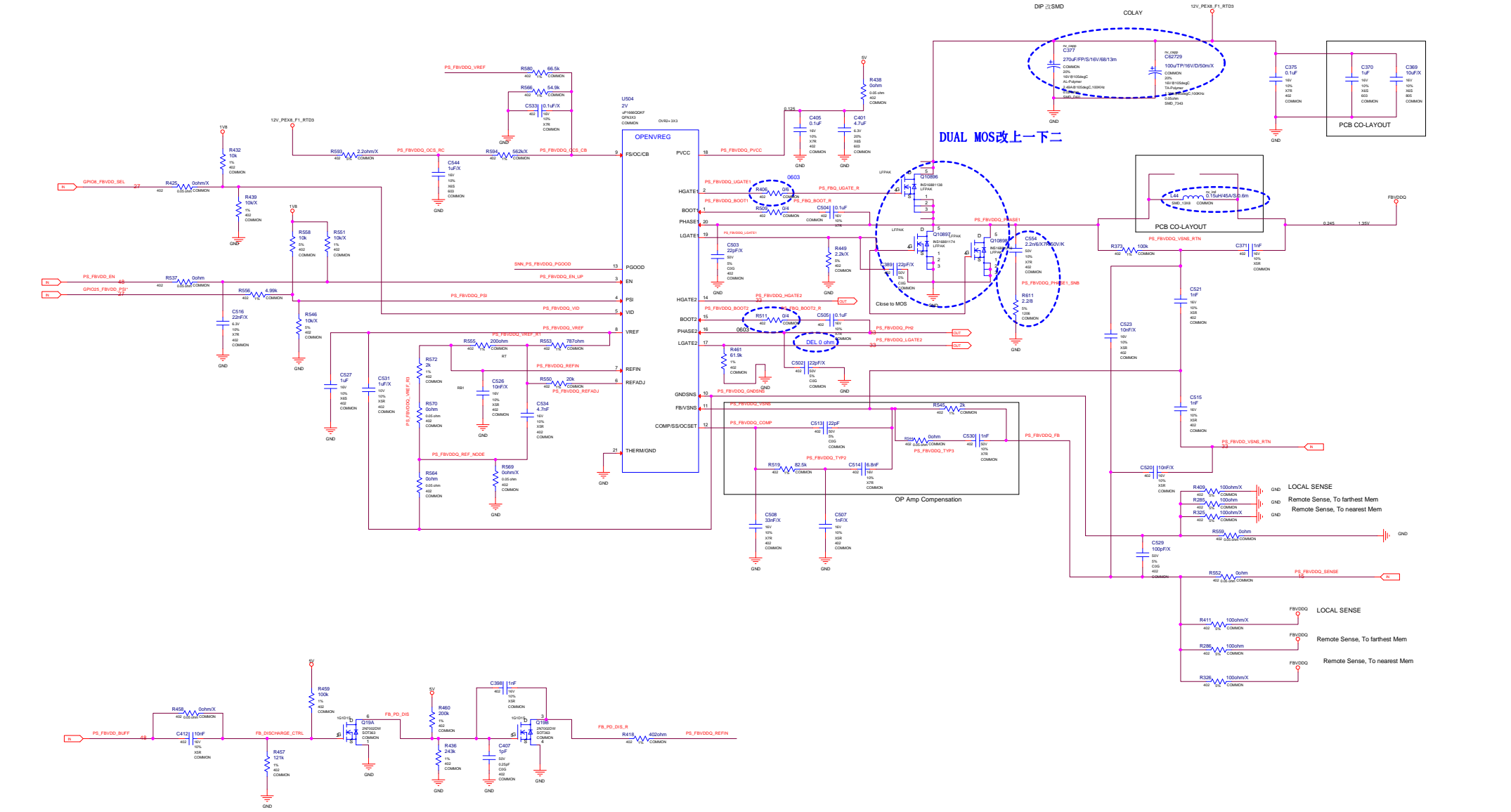
RED DRIVE

GREEN DRIVE

BLUE DRIVE

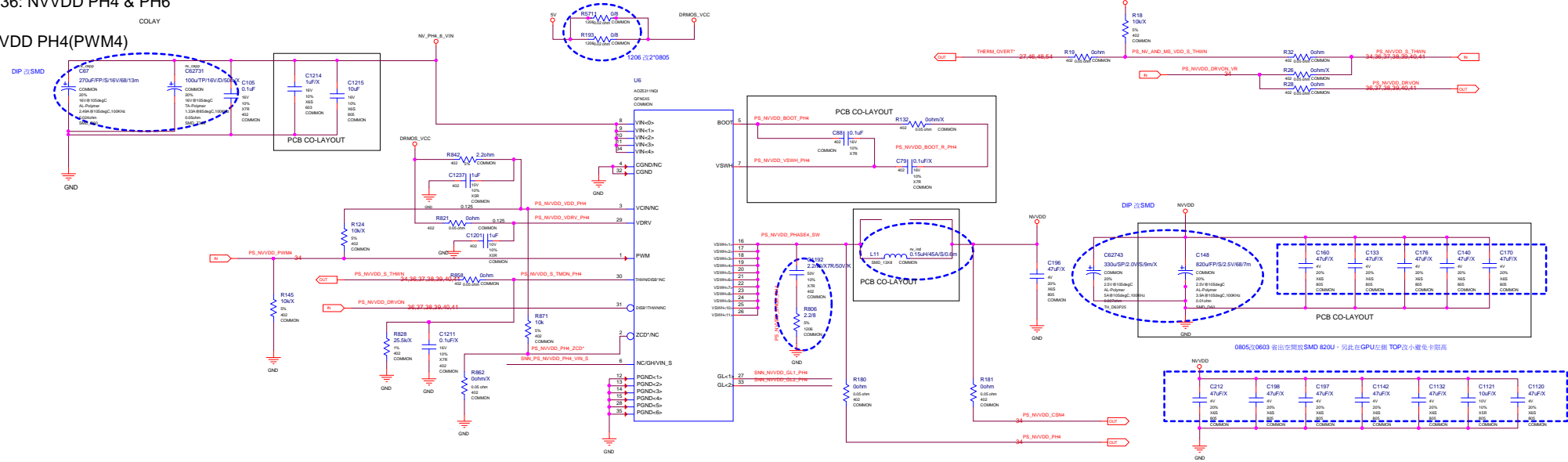


$$0.6V^*(1+10K/16.9K)=0.955V$$


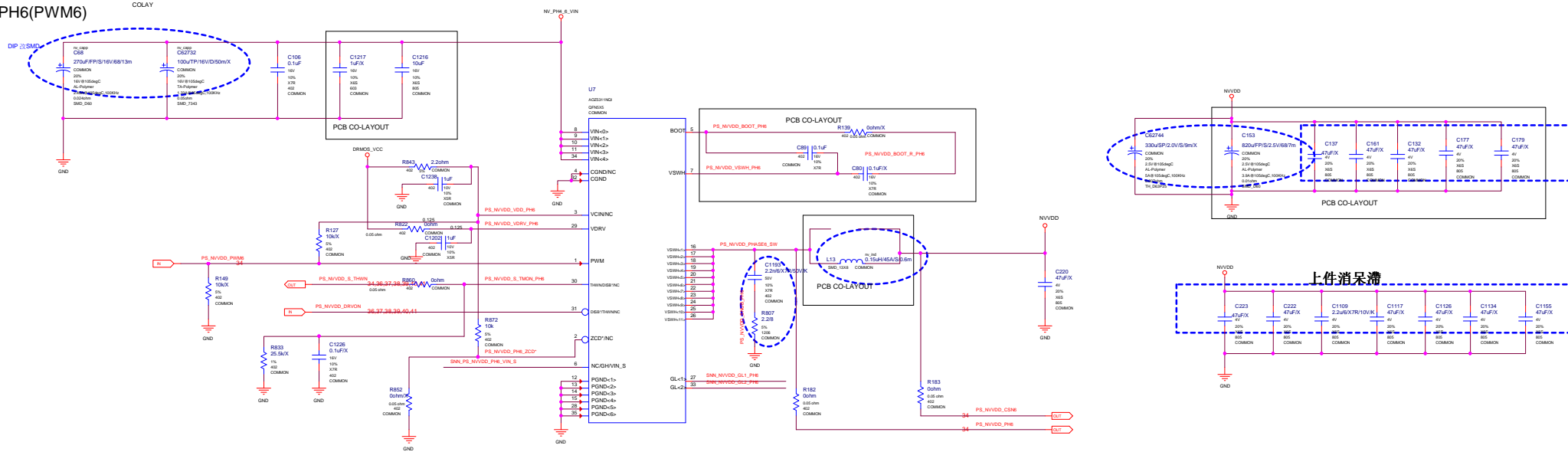


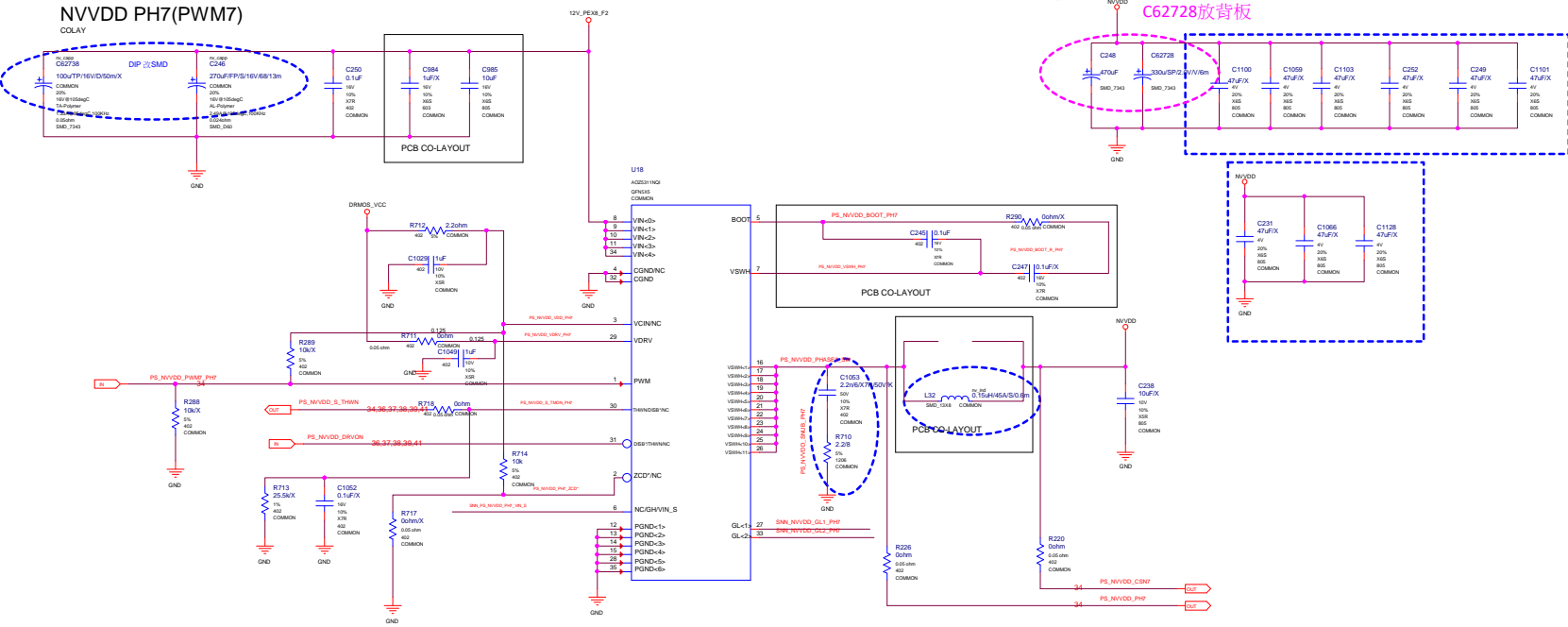
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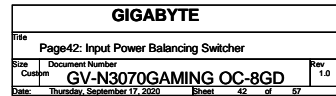
NVVDD PH4(PWM4)

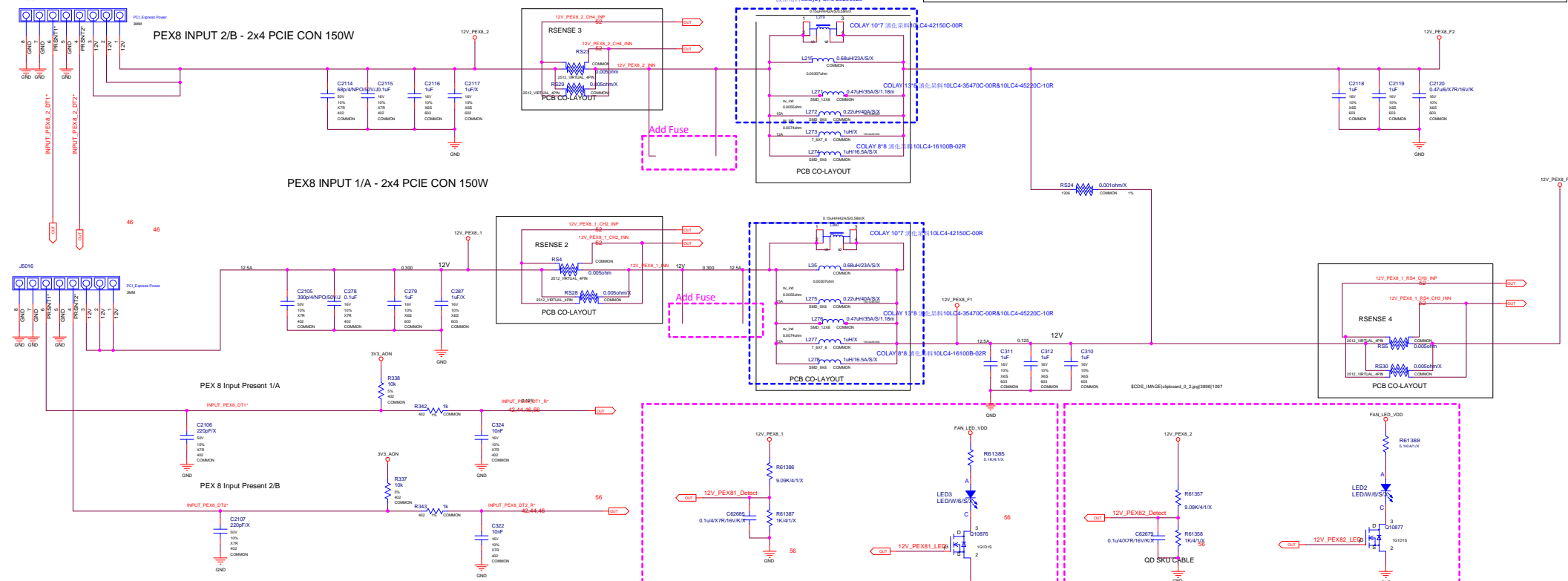
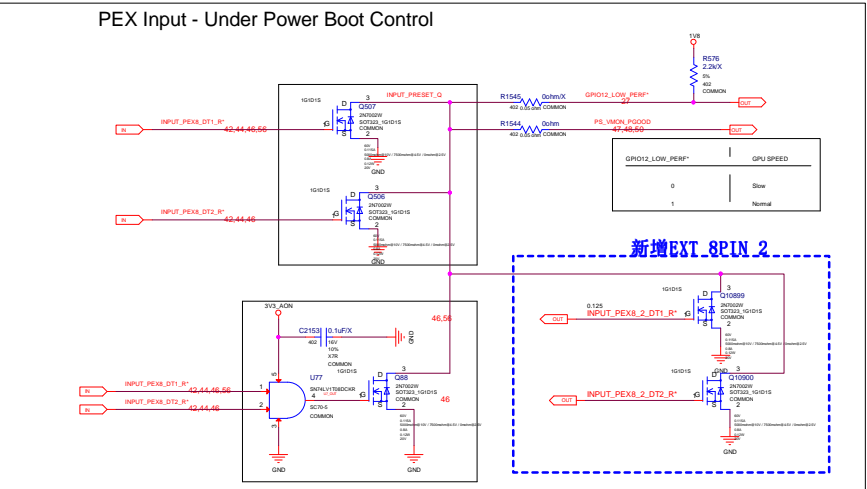
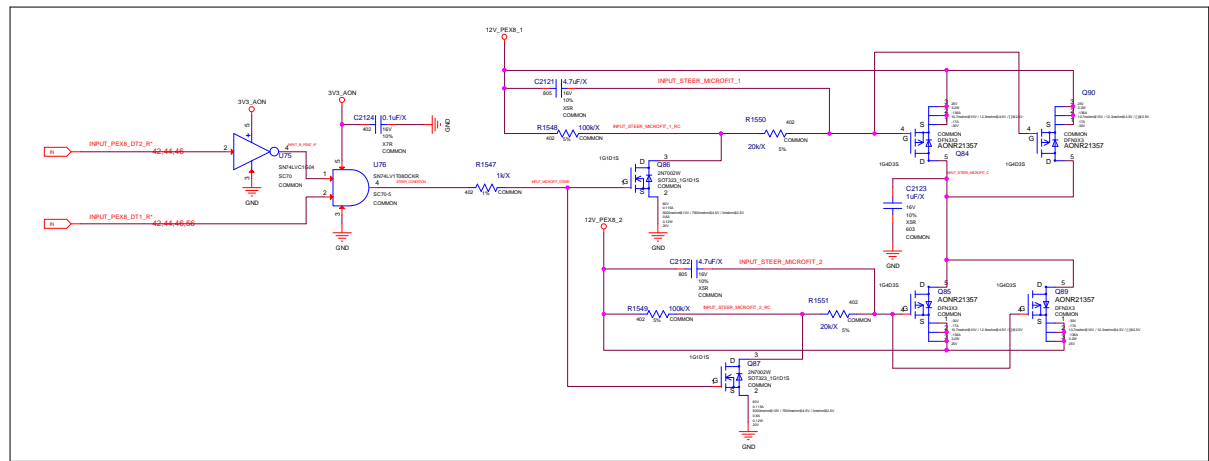


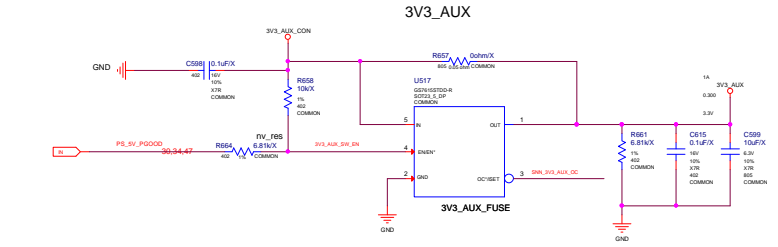
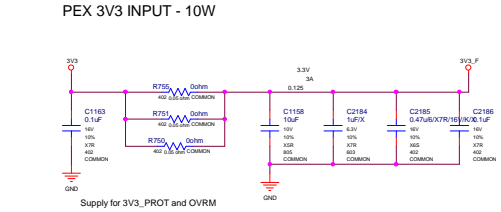
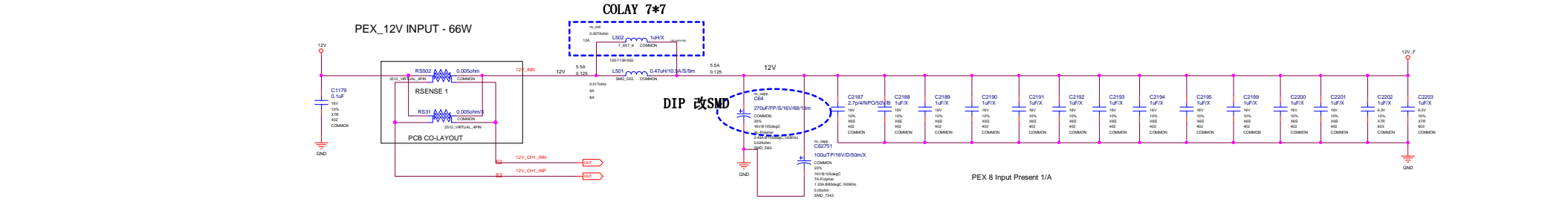
NVVDD PH6(PWM6)

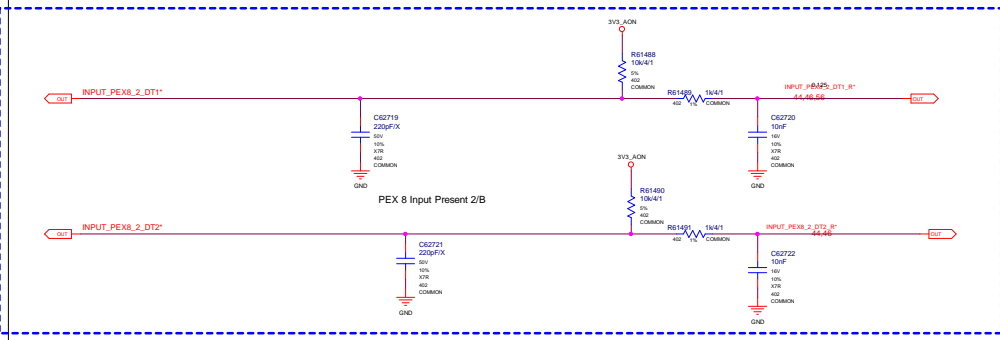




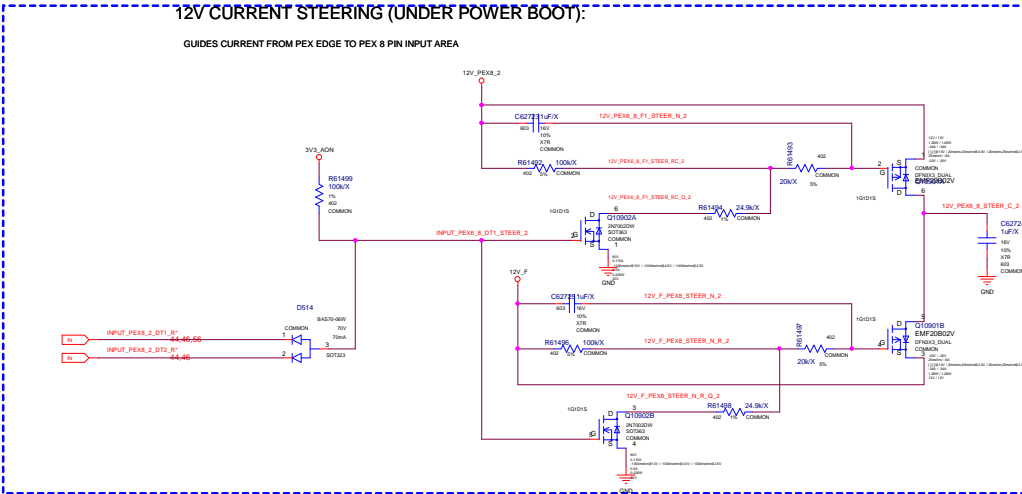








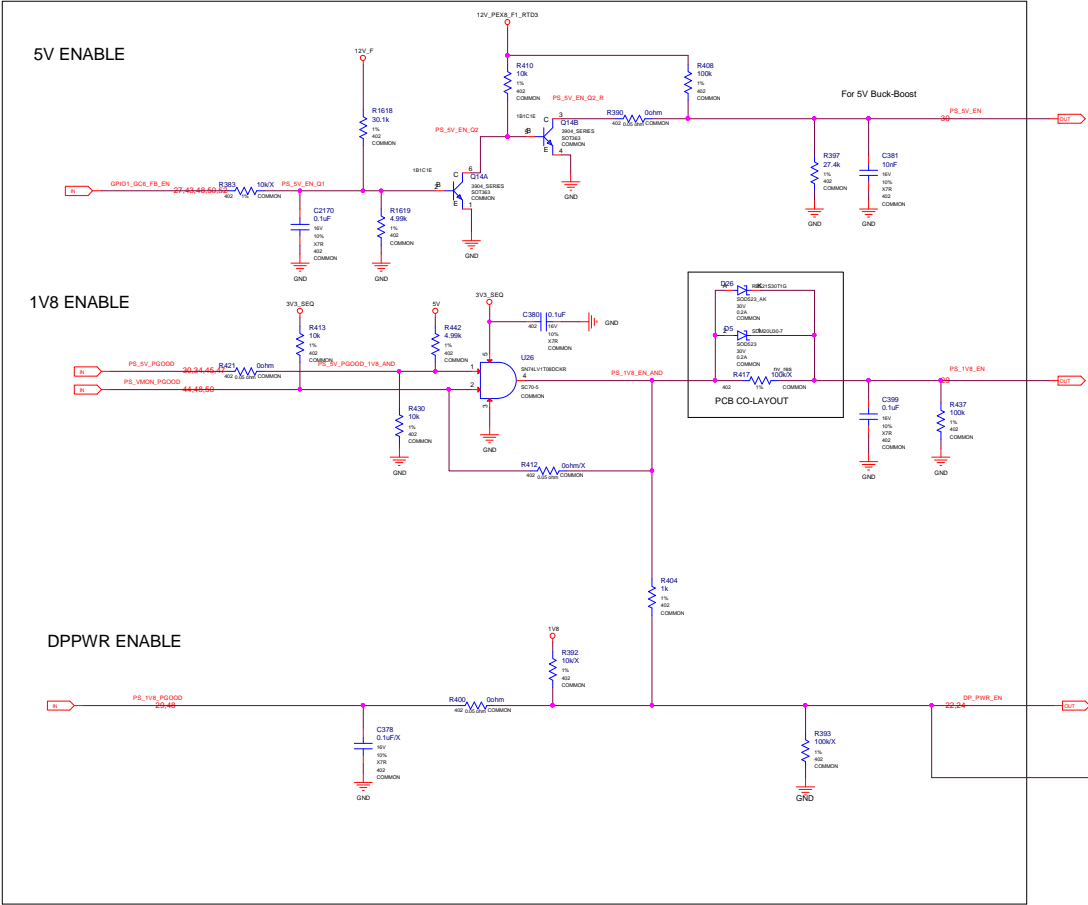
ADD PEX8_2



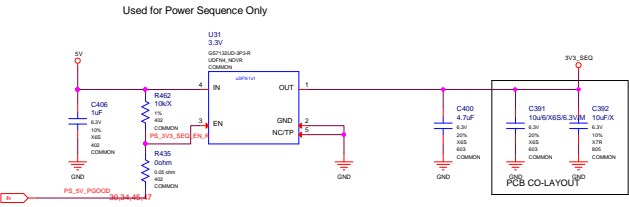
12V CURRENT STEERING (UNDER POWER BOOT):

12V CURRENT STEERING (UNDER POWER BOOT):

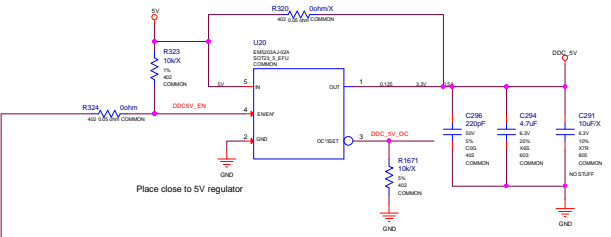
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



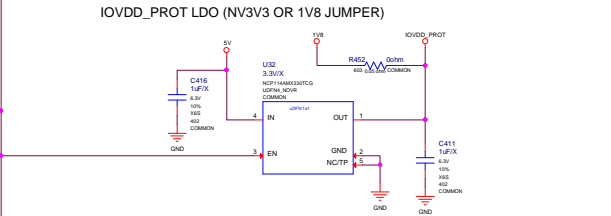
3V3_SEQ



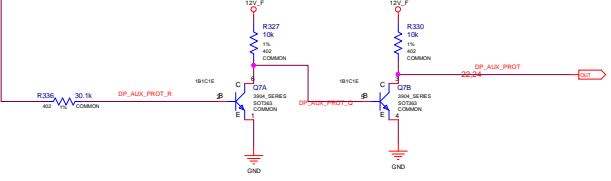
DDC_5V

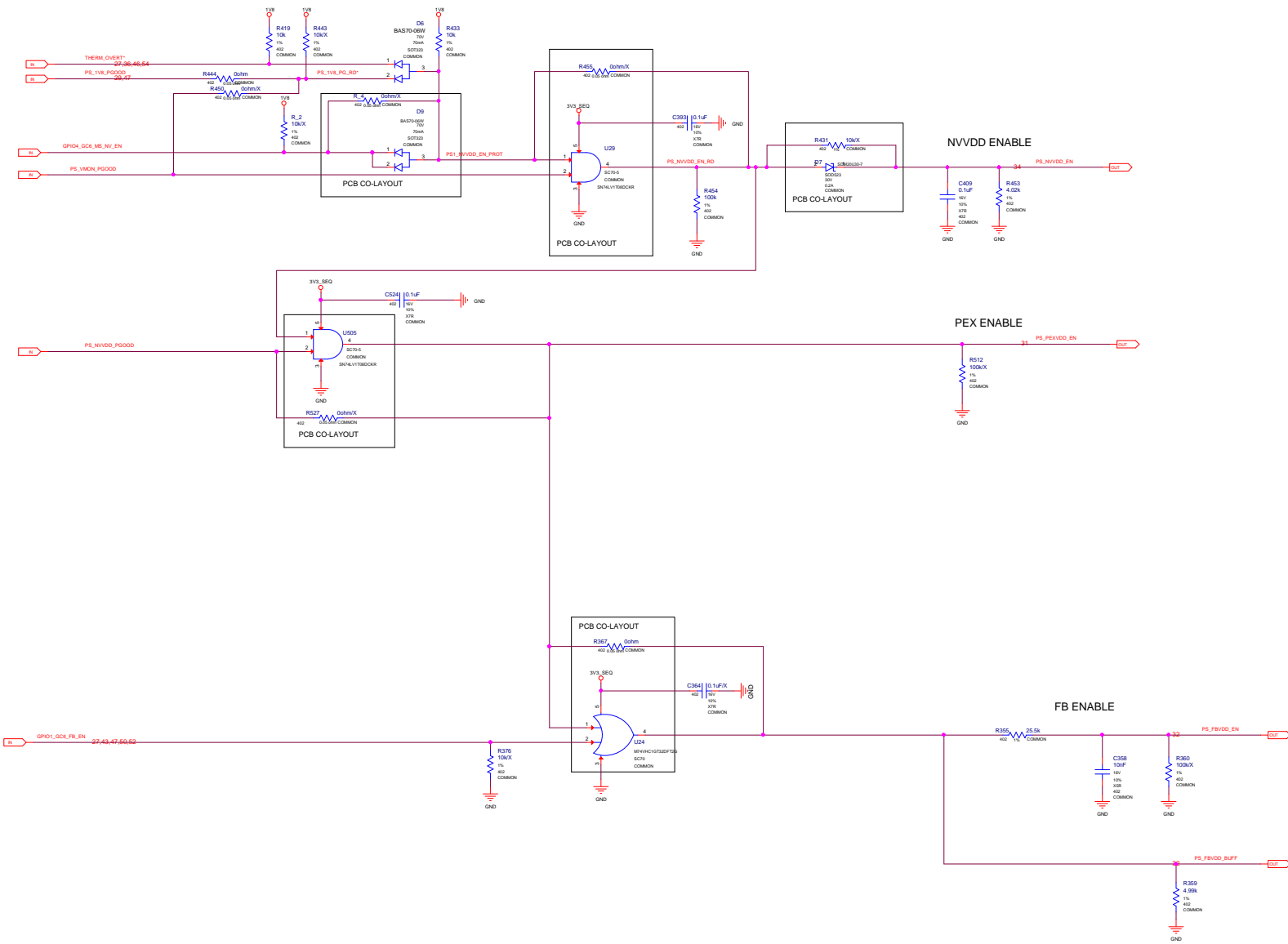


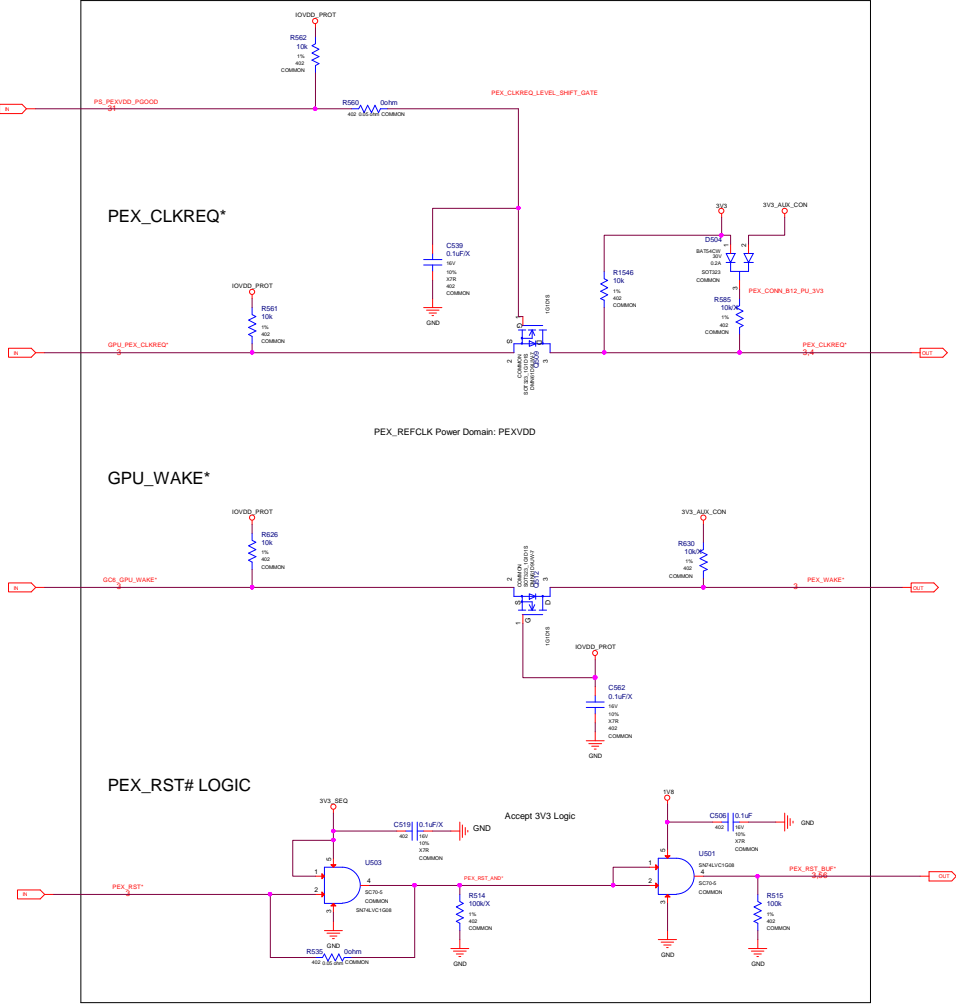
IOVDD_PROT

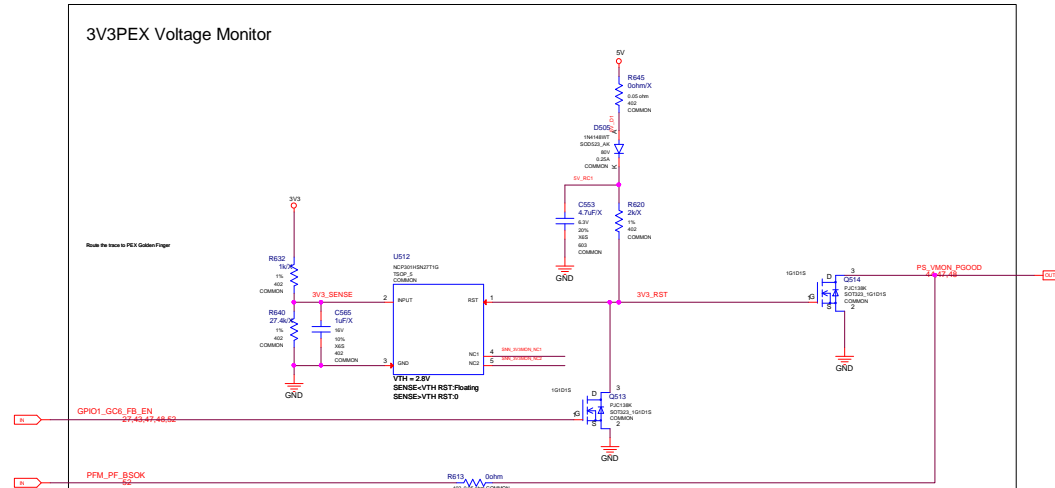


DP_AUX PROTECTION









BOM Configuration

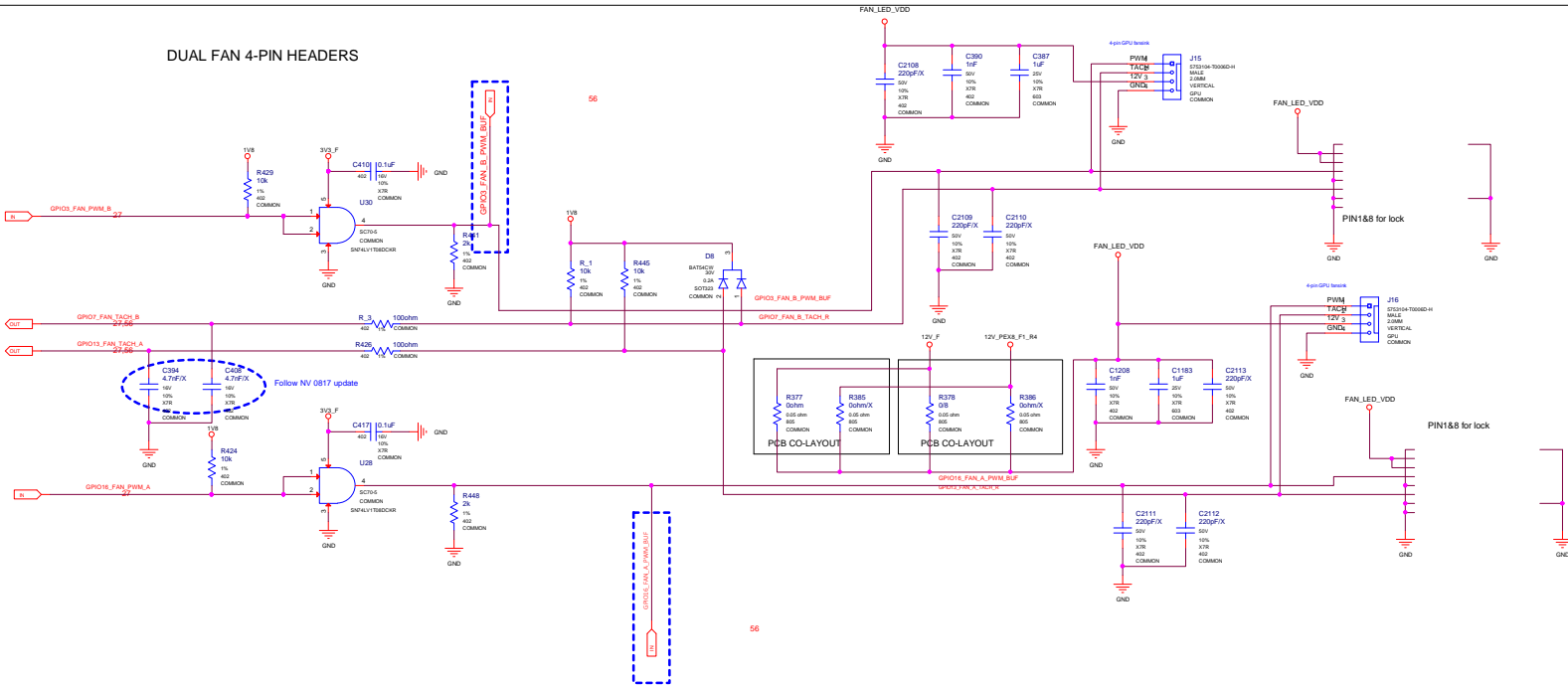
OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(↑) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence, Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK0	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS



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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

